REMARKS

The foregoing amendments and the following remarks are responsive to the April 9, 2003 Office Action. Claims 1, 2, and 6-8 are cancelled herein, Claim 3 is amended herein, and Claims 10-11 are added herein. Claims 5 and 9 were previously cancelled and Claim 4 remains as filed. Thus, Claims 3, 4, 10, and 11 are presented for further consideration. Please enter the amendments and reconsider the claims in view of the following remarks.

Comments on Preliminary Amendment Mailed May 12, 1999

On May 12, 1999, Applicants mailed a "Preliminary Amendment" which amended Claims 1 and 3. With regard to Claim 3, this Preliminary Amendment inserted the phrase "at least" before the words "two parallel circuits" in line 6, so that Claim 3 referred to "at least two parallel circuits, at least one circuit having said memory element (M_j)." However, the Preliminary Amendment misidentified the second use of the phrase of "at least" as the inserted language rather than the first use of the phrase.

In addition, with regard to Claim 3, the Preliminary Amendment included a typographical error in which the phrase "columns and rows" was replaced with the phrase --rows and columns-- in line 1, but without any indications (e.g., underlined text, bold and bracketed text, or struckthrough text) that such a replacement was made. The present Response ignores this typographical error of the Preliminary Amendment, and returns the phrase to its original form.

Furthermore, with regard to Claim 3, the Preliminary Amendment indicated that the phrase "the two parallel circuits being connected through a switch ($S6_j$) with the same input of said amplifying element (A_j)" was being deleted. However, Claim 3 has never included this phrase, so this deletion was a nullity.

Applicants regret any confusion which resulted from these errors.

Response to Rejection of Claim 7 Under 35 U.S.C. § 112, Second Paragraph

In the April 9, 2003 Office Action, the Examiner rejects Claim 7 under 35 U.S.C. § 112, second paragraph as being indefinite. As described herein, Applicants have cancelled Claim 7 without prejudice.

Response to Rejection of Claims 1-4 and 6-8 Under 35 U.S.C. § 103(a)

In the April 9, 2003 Office Action, the Examiner rejects Claims 1-4 and 6-8 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,434,619 to Yonemoto in view of U.S. Patent No. 5,311,320 to Hashimoto.

Claims 1, 2, and 6-8

As described herein, Applicants have cancelled Claims 1, 2, and 6-8 without prejudice.

Claim 3

The Examiner states that Yonemoto discloses all the limitations of Claim 3, except for the common output amplifier. The Examiner further states that Hashimoto discloses an image sensor with an output differential amplifier and that it would have been obvious to one of ordinary skill in the art at the time of the invention to have made Yonemoto's subtractor a differential amplifier to subtract one signal from another. The Examiner relies on Hashimoto's disclosure of an image sensor with an output differential amplifier for this limitation.

Applicants have amended Claim 3 as described herein. Applicants submit that the combination of Yonemoto and Hashimoto does not disclose all the limitations claimed in amended Claim 3. Amended Claim 3 makes clear that the amplifying element (A_j) is a column amplifying element, i.e., all pixels of one column are connected to a common pixel output line having such a column amplifying element, and thereafter all columns are connected to a common output amplifier (D). This means that such a column amplifying element is provided for each column of pixels. The column amplifying elements are different from the common output amplifier (D), which is provided in common to all columns of pixels, i.e., all pixel signals ultimately pass through the common output amplifier (D). Support for this wording can be found on page 12, lines 12-13 of the present application.

Furthermore, in amended Claim 3, a feature is added which describes a further switch being present between each column amplifying element and the common output amplifier. Support for this feature can be found in Fig. 2, where the further switches are clearly shown as the switches X_1, X_2, X_N.

Yet another feature is added in amended Claim 3, which restricts the image sensor to CMOS or MOS sensors. Support for this restriction can be found on page 1, lines 12-14 of the present application, where it is said that the present invention relates to solid state imaging devices manufactured in a CMOS- or MOS-technology.

Amended Claim 3 as discussed above distinguishes over Yonemoto. In Yonemoto, as can be seen in Fig. 3 thereof, an image sensor is described comprising an array of columns and rows of pixels, all the pixels of one column of the array being connected to at least one common pixel output line having at least one memory element.

However, Yonemoto does not disclose that the at least one common pixel output line has at least one column amplifying element. Contrary thereto, the output line common to all pixels of a column is split into two parallel circuits, each of those parallel circuits bringing either an image signal or a noise signal to one of two output lines, each of those output lines comprising an amplifying element 7a, 7b.

Those amplifying elements 7a, 7b are not column amplifying elements but are common to all columns, i.e., they are common output amplifiers. Therefore, Yonemoto does not describe that the at least one column pixel output line has at least one column amplifying element.

In Yonemoto, contrary to the present invention, pixel signals and noise signals are each sent through a different amplifying element 7a, 7b, and therefore any offset of the amplifying elements is introduced in the signals, which is not cancelled out as is the case in the present invention (see description page 10, line 29 - page 11, line 5). Yonemoto does not suggest a read-out scheme for image sensors that suppresses the effects of non-uniformities caused by variations in the output amplifiers.

This problem is overcome by the present invention as recited in amended Claim 3, in which a column amplifying element is provided, which is a voltage buffer or buffer amplifier as cited on page 10, line 4, through which both the pixel signal and the noise signal are sent, i.e., the same offset value is applied to the pixel signal as to the noise signal. When the noise signal is subtracted from the pixel signal in common output amplifier D, the offset introduced by the column amplifier, which offset was present in both signals, is cancelled out.

In view of the above, amended Claim 3 is considered novel and inventive over Yonemoto.

Amended Claim 3 also distinguishes over U.S. Patent No. 5,339,106 to Ueno. In Ueno, more particularly in the prior art part referred to in Fig. 1 thereof, an image sensor is described comprising an array of columns and rows of pixels, all the pixels of one column of the array being connected to at least one common pixel output line having at least one memory element and at least one column amplifying element.

It can be seen from Fig. 1 of Ueno that the common pixel output line is divided through switches Qh1, Qh2 in two parallel circuits, at least one of those circuits, and in the embodiment illustrated both parallel circuits having a memory element C1, C2. The two parallel circuits are connected through a switch Qh3, Qh4 with the same input of the column amplifying element.

The column amplifying element in Fig. 1 of Ueno comprises a buffer amplifier Qh5, which is a bipolar transistor, a MOS transistor Qh9, and a MOS transistor Qh6. By making the transistor Qh6 conductive, transistor Qh5 is connected to the ground, goes out of its normal working area and becomes a high impedance. MOS transistor Qh9 does not behave as a switch, as its gate is connected to a DC voltage source. The switching is provided by the combined operation of Qh6 and Qh5.

Fig. 1 of Ueno thus shows an image sensor in which the amplifying element is a bipolar transistor. This is contrary to the present invention, in which the image sensor is made in MOS- or CMOS-technology. Thus, the device of Ueno requires a complex manufacturing process due to the combination of technologies required.

According to the present invention, the amplifying element of Fig. 1 of Ueno has not been simply replaced by a CMOS amplifier, but furthermore, a further switching element X_j has been added in at each column, between the column amplifying element and the common amplifier. This distinguishes the circuit of the present invention from Fig. 1 of Ueno.

By introducing the supplementary switches X_j according to the present invention, the output capacitance of each column amplifier is decoupled from the common output line or bus on which the common amplifying element D is present. In Ueno, all common amplifiers remain connected to the common bus at all times, even when driven in saturation. Each column amplifying element in Ueno is connected via a low capacitance, e.g., a few fF, to the bus. This will slow down the overall operation of the image sensor.

Furthermore, the Ueno column amplifier is a source follower which requires that at the end of the common bus, a load resistance is connected to the ground. Therefore, voltage drops and series currents are created over and in the common bus. These voltage drops are being felt differently for every column, as the distance from a column connection point on the bus to the end of the bus is different for every column, and thus the series resistance of the bus itself is different for each column. Therefore, the amplifiers of each column have to be driven slightly differently.

With the solution according to the present invention, incorporating a supplementary switch X_j, the bus may be a simple metal line, and no resistive load is required. All columns can be treated as being the same.

In view of the above, the circuit of the present invention is novel over Ueno. The circuit of the present invention is not a simple change of the bipolar amplifier into a CMOS amplifier, therefore the present invention is considered to be inventive over Ueno.

Applicants have also considered the other prior art documents made of record but not relied upon by the Examiner, but was not able to identify any document which would be closer to the present invention than the documents discussed above.

Claim 4

Claim 4 depends from amended Claim 3. Thus, Claim 4 includes all the limitations of amended Claim 3, as well as recites further limitations of particular utility. Therefore for the above-stated reasons with regard to amended Claim 3, Applicants submit that Claim 4 is patentably distinguished over Yonemoto in view of Hashimoto. Applicants respectfully request that the Examiner withdraw the rejection of Claim 4 and pass Claim 4 to allowance.

Comments on New Claims 10-11

New Claims 10 and 11 each depends from amended Claim 3, so each includes all the limitations of amended Claim 3, as well as recites further limitations of particular utility. For the reasons stated above in relation to amended Claim 3, Applicants submit that new Claims 10-11 are patentable and respectfully request that the Examiner pass Claims 10-11 to allowance.

Summary

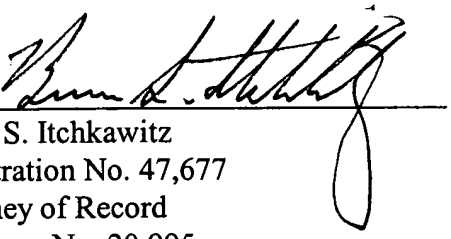
In view of the foregoing amendments and remarks, Applicants respectfully submit that Claims 3, 4, 10, and 11 are in condition for allowance, and Applicants respectfully request prompt allowance of Claims 3, 4, 10, and 11.

Please charge any additional fees, including any fees for additional extension of time, or credit overpayment to Deposit Account No. 11-1410.

Respectfully submitted,

KNOBBE, MARTENS, OLSON & BEAR, LLP

Dated: 7/9/03

By: 

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